

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Farid Nemati, et al.) Examiner: Unknown
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Serial No.: divisional of 10/282,331) Group Art Unit: Unknown
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Filed: herewith))
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For: Carrier Coupler for Thyristor-Based))
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))
Semiconductor Devices)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on the attached Form PTO-1449 is information known to applicant. Each reference cited herein was previously cited in parent applications and a copy of each reference was provided to the Examiner, or cited by the Examiner in an Office Action. No additional copies of the references are being submitted with this paper, but will be furnished upon the Examiner's request.

Applicants respectfully request that the listed information be considered by the Examiner and be made of record in the above-identified application. If form PTO-1449 is enclosed, the Examiner is requested to initial and return it in accordance with MPEP 609.

This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in section 1.56.

Respectfully submitted,

Date: February 23, 2004



Hark C. Chan (Reg. No. 35,477)

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Substitute for form 1449/PTO

Complete if Known**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Sheet 1 of 3

Application Number	
Filing Date	
First Named Inventor	Farid Nemati
Art Unit	
Examiner Name	
Attorney Docket Number	C033-D-1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (<i>if known</i>)			
		US- 6,229,161	5-8-2001	Nemati et al.	
		US- 6,104,045	8-15-2000	Forbes et al.	
		US- 4,797,373	1-10-1989	Malhi et al.	
		US- 6,225,165	5-1-2001	Noble, Jr. et al.	
		US- 5,528,062	6-18-1996	Hsieh et al.	
		US- 5,132,767	7-1992	Ogura et al.	
		US- 6,084,274	7-2000	Mukai et al.	
		US- 5,600,160	2-1997	Hvistendahl	
		US- 6,545,297	4-2003	Nobel, Jr. et al.	
		US- 6,583,452	6-2003	Cho et al.	
		US- 4,395,723	7-1983	Harari	
		US- 2002/0190265 A1	12-2002	Hsu et al.	
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (<i>if known</i>)				
		Japan 3-16089	1-1991	Sato et al.		

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	
				Filing Date	
				First Named Inventor	Farid Nemati
				Art Unit	
				Examiner Name	
Sheet	2	of	3	Attorney Docket Number	C033-D-1

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
		K. DeMeyer, S. Kubicek and H. van Meer, Raised Source/Drains with Disposable Spacers for sub 100 nm CMOS Technologies, Extended Abstracts of International Workshop on Junction Technology 2001.			
		Mark Rodder and D. Yeakley, Raised Source/Drain MOSFET with Dual Sidewall Spacers, IEEE Electron Device Letters, Vol. 12, No. 3, March 1991			
		Yang-Kyu Choi, Daewon Ha, Tsu-Jae King and Chenming Hu, Nanoscale Ultrathin PMOSFETs with Raised Selective Germanium Source/Drain, IEEE Electron Device Letters, Vol. 22, No. 9, September 2001.			
		N. Lindert, Y. K. Choi, L. Chang, E. Anderson, W. C. Lee, T. J. King, J. Bokor, and C. Hu, Quasi-Planar FinFETs with Selectively Grown Germanium Raised Source/Drain, 2001 IEEE International SOI Conference, 10/2001			
		T. Ohguro, H. Naruse, H. Sugaya, S. Nakamura, E. Morifuji, H. Kimijima, T. Yoshitomi, T. Morimoto, H.S. Momose, Y. Katsumata, and H. Iwai, High Performance RF Characteristics of Raised Gate/Source/Drain CMOS with Co Salicide, 1998 Symposium on VLSI Technology Digest of Technical Papers			
		Hsiang-Jen Huang, Kun-Ming Chen, Tiao-Yuan Huang, Tien-Sheng Chao, Guo-Wei Huang, Chao-Hsin Chien, and Chun-Yen Chang, Improved Low Temperature Characteristics of P-Channel MOSFETs with Si1-xGex Raised Source and Drain, IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001			
		Nemati, Farid, and Plummer, James, D., "A Novel High Density, Low voltage SRAM Cell with a Vertical NDR Device," VLSI Technology Technical Digest, June 1998			
		Stanley Wolf Ph.D. and Richard N. Tauber Ph.D., Silicon Processing for the VLSI Era, Vol. 1, 1986, page 285-286			
		Nemati, Farid, and Plummer, James, D., "A Novel Thyristor-Based SRAM Cell (T-RAM) for High Speed, Low Voltage, Giga-Scale Memories," International Electron Device Meeting Technical Digest, 1999			

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		NN80081017, Single Thyristor Static Memory and its Fabrication, 8/1980, IBM, Technical Disclosure Bulletin, Vol. 23, Issue 3, pp. 1017-25			
		Zeng et al., Effect of Carrier Lifetimes on Forward Characteristics of MOS-Controlled Thyristors, 6/1995, IEE, IEE Proc.-Circuits Devices Syst., Vol. 142, No. 3, pp. 205-07			
		Kim et al., Realization of a Fast Switching Thyristor by Local Carrier Lifetime Control, 5/2002, IEEE, Proc. 23rd International Conference on Microelectronics, Vol. 1, pp. 193-96			

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